Analysis of Single Wall Carbon Nanotube Interconnects & Comparison with Copper Interconnects at Different Technology Nodes

Prashant Gupta, Gagnesh Kumar

Abstract— This paper investigates the performance of the bundle of Single wall Carbon Nanotubes (SWCNT) for low-power and high-speed interconnects for future VLSI applications. The power dissipation and delay of SWCNT bundle interconnects are examined and compared with that of the Cu interconnects at the different technology (16nm, 22nm, 32nm & 45nm) nodes for both intermediate and global interconnects. The results show that SWCNTs bundle consume less power and also faster than Cu for intermediate and global interconnects. It is concluded that the Metallic SWCNT has been regarded as a viable candidate for intermediate and global interconnects in future technologies.

Index Terms— ***Carbon nanotube, SWCNT, Low power,High speed, Delay,Technology, Global and intermediate interconnects***

1 Introduction

With the advancement of VLSI technology, the device and their interconnects dimensions have been shrunk from micrometer-to-submicrometer-to-nanometer regime. As the fabrication technology move to very deep sub-micron (VDSM) design region, the intrinsic gate delay tends to decrease significantly. In contrast, the interconnects length and overall chip size on a chip tend to increase, mainly due to increasing chip complexity; thus, the significance of interconnects delay increases in VDSM technologies. In deep submicron technologies interconnects associated with parasitic such as capacitance and inductance along with resistance. As the dimensions of the devices and their interconnections reach to the nanometer level, the bulk properties of the materials cannot be applied and the devices must be analyzed in atomic level.

As interconnects feature size minimized, copper resistivity increases due to grain boundary and surface scattering and also surface roughness [1]. The steep rise in parasitic resistance of copper interconnects poses serious challenge for interconnect delay. According to ITRS, the Cu wires are becoming more and more vulnerable to Electromigration because of rapid increase in current density which causes the electromigration [2]. All these factors result in degraded interconnect performance with each technology generation which conflicts with the high performance requirement, such as low power, low interconnect delay and reliability of VLSI circuits in VDSM. In order to overcome the limitation of copper interconnects, bundle of CNTs have been proposed as possible replacement for copper interconnects in future technologies due to its higher conductivity and current carrying capabilities without Electromigration problem.

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However, the resistance of an isolated SWCNT is quite high (of the order of 6.45 KΩ) [3].to reduce the resistance of SWCNT interconnects necessitates the use of a bundle of SWCNTs. A SWCNT consists of one graphene shell and has electron mean free paths of the order of a micron [3] and achieves ballistic transport over long lengths.

The paper is organized in the following manner. Section II explained types of interconnect and its effect on performances of the circuit. Electrical model of SWCNT is described in section III of the paper. Simulation results and comparison of SWCNT interconnect with conventional Cu interconnect has been reported in section IV and section V concludes the paper.

2 INTERCONNECTS

2.1 Global Interconnects

Global interconnects provides power supply, clock distribution and long distance communication between functional blocks and deliver ground to all functions in a chip . Global interconnect lengths can be the order of millimeters. Low resistive material like aluminum, copper are generally use in global interconnect to reduce the overall delay. Repeaters are normally inserted in order to reduce the delay and increase the drive capability [4].With the advancement of technology global interconnect length increases due to increase in chip complexity. The comparison of delay and power for global interconnect length of 1000μm between SWCNT bundle and Cu at different technology nodes are shown in fig.4.2 and fig. 4.4.

2.2 Intermediate Innterconnects

The length of intermediate level of interconnects are shorter than that of global interconnects, despite being shorter in length as compared to the global interconnect, intermediate interconnect still require repeaters. All the parameters for intermediate interconnect used for simulation are used from ITRS 2011as mention in table I. Fig 4.1 and 4.3 show that delay and power comparison of SWCNT and Cu for intermediate interconnect length of 100um for different technology nodes.

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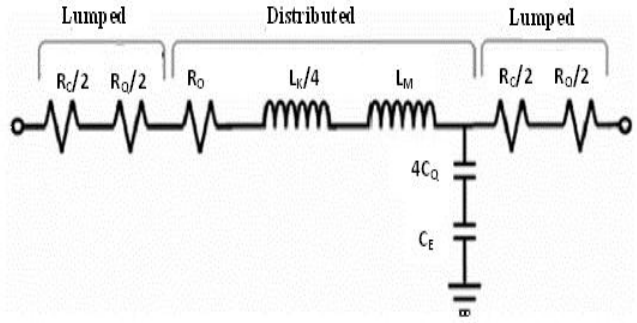

Fig. 1. Equivalent circuit of SWCNT [5]

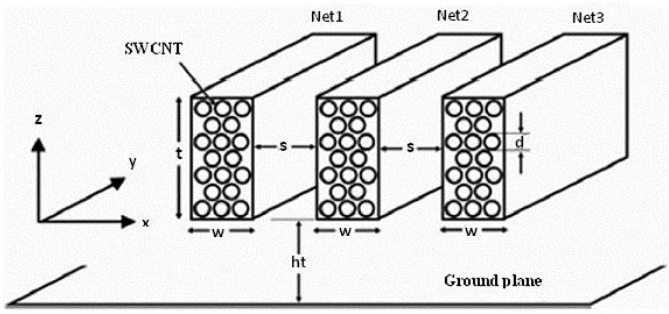

Fig.2. Interconnect structure using swcnt bundle [5]

3 ELECTRICAL MODEL OF SWCNT

SWCNTs bundle can be model as a VLSI interconnect, the electrical model of SWCNT bundle consists of Resistance ,Inductance and capacitance [4] .To extract the *RLC* equivalent circuit for the CNT-based interconnects, we use the equivalent circuit of SWCNT proposed by Burke [7, 8], as shown in Fig. The electrical circuit parameters of SWCNT are explained as follow

3.1 Resistance of SWCNT

The resistance of a SWCNT can be modelled in three parts
i) Contact resistance (R_C) ii) Quantum resistance (R_q)
iii) Ohmic resistance (R_O) [6]-[8]

$$R_{CNT} = R_C + R_Q + R_O \;\; for\; l_{CNT} > \lambda \tag{1}$$

$$R_{CNT} = R_C + R_Q \;\; for\; l_{CNT} \leq \lambda \tag{2}$$

Where l_{CNT} is the length of SWCNT and λ is the mean free path (MFP) of electron.

The quantum and ohmic resistances are given by

$$R_Q = \frac{h}{4e^2} \tag{3}$$

$$R_O = R_Q.\left(\frac{l_{CNT}}{\lambda}\right) \tag{4}$$

respectively, where h and e are the Plank's constant and the electronic charge respectively.

3.2 Inductance of SWCNT

Inductance of SWCNT is modelled in two parts [6]-[8]
i) Kinetic inductance (L_K) ii) Magnetic inductance (L_M)
The kinetic Inductance is given by expression

$$L_K = \frac{h}{2e^2 v_F} \tag{5}$$

where v_F is the Fermi velocity which is usually taken as 8×10^5 m/s for CNT. As there are four conducting channels in SWCNT, the effective kinetic inductance is $L_K/4$.

Magnetic inductance (L_M) is given by

$$L_M = \left(\frac{\mu}{2\pi}\right).\ln\left(\frac{ht}{d}\right) \tag{6}$$

Where *ht* is the height of the CNT from ground plane and *d* is the diameter of the CNT.
It is observed that the magnetic inductance is insignificant as compared to the kinetic inductance. Therefore, the inductance of SWCNT is approximately given by $L_{CNT} \approx L_K/4$.

3.3 Capacitance of Isolated SWCNT

The capacitance of CNT is modeled by two parts [6]-[8]
i) Electrostatic capacitance (C_e) ii) Quantum capacitance
The expression of electrostatic capacitance is given by

$$C_E = \frac{2\pi\varepsilon}{\ln(ht/d)} \tag{7}$$

Quantum capacitance (C_Q) is given by equation

$$C_Q = \frac{2e^2}{hv_F} \tag{8}$$

where v_F is the Fermi velocity which is usually taken as 8×10^5 m/s for CNT.

3.4 RLC Parameters of a SWCNT Bundle

Isolated SWCNT has very large intrinsic resistance (6.45 kΩ) due to this, a bundle of SWCNT is proposed for the interconnects. However, due to lack of control on the chirality of SWCNTs bundle, a bundle normally consists of both metallic and semiconducting SWCNT bundle. If *w* and *t* are the interconnect width and thickness, respectively, the number of SWCNTs along the *x* and *z* (see Fig. 5) direction can be expressed as [6]-[8]

$$N_x = \frac{(w-d)}{x} \tag{9}$$

$$N_z = \frac{2(t-d)}{(\sqrt{3}x)} + 1 \tag{10}$$

where *d* is the diameter of SWCNT and *x* is the inter-SWCNT

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distance. We assume densely packed SWCNT bundle. For the densely packed bundle, the inter-SWCNT distance is *d*. Using the expressions of n_x and n_z, the total number of CNTs in a bundle can be expressed as [5]

$$N_{CNT} = N_x N_z - \frac{N_z}{2} \quad if\ N_z\ is\ even \tag{11}$$

$$N_{CNT} = N_x n N_z - \frac{(N_z-1)}{2} \quad if\ N_z\ is\ odd \tag{12}$$

As the bundle is consist of number of SWCNTs in parallel, the effective capacitance, resistance, and inductance are given by parallel combination of capacitance, resistance, and inductance of the individual SWCNT. Therefore, the resistance (R_b), inductance(L_b), and capacitance (C_b) of a SWCNTs bundle of length l_{CNT} can be expressed as [6]-[8]

$$R_b = \frac{R_{CNT}}{N_{CNT}} \tag{13}$$

$$L_b = \frac{l_{CNT}.L_{CNT}}{N_{CNT}} \tag{14}$$

$$C_b = l_{CNT}.\frac{C_Q^b\, C_E^b}{(C_Q^b + C_E^b)} \tag{15}$$

Where C_Q^b and C_E^b are the quantum and electrostatic capacitances of the SWCNT bundle which are given by

$$C_Q^b = C_Q^{CNT}.N_{CNT} \tag{16}$$

$$C_E^b = 2C_{En} + \frac{N_x-2}{2}C_{Ef} + \frac{3(N_z-2)}{5}C_{En} \tag{17}$$

where C_{En} is the capacitance calculated assuming ground plane at a distance equal to spacing (*s* in Fig.2) between the interconnects and capacitance C_{Ef} is calculated assuming ground plane at a distance equal to spacing plus width of interconnects ($s + w$ in Fig. 2).

TABLE I
INTERCONNECT PARAMETERS (ITRS 2011)

	INTERMEDIATE LEVEL				GLOBAL LEVEL			
Technology	***45 nm***	***32 nm***	***22 nm***	***16 nm***	***45 nm***	***32 nm***	***22 nm***	***16 nm***
Width (nm)	45	32	22	16	67.5	48	32	24
$A/_R$	1.8	1.9	2	2	2.3	2.4	2.5	2.6
Height (nm)	81	60.8	44	32	155.25	115.2	80	62.4
t_{ILD} (nm)	76.8	54.4	39.6	28.8	148.5	110.4	76.8	60
ρ_{Cu} (μΩcm)	4.08	4.83	6.01	7.34	3.1	3.52	4.2	4.93
K_{ILD}	2.6	2.3	2.0	1.7	2.6	2.3	2.0	1.7

TABLE II
RLC PARAMETERS OF Cu & SWCNT AT DIFFERENT TECHNOLOGY NODES FOR INTERMEDIATE INTERCONNECT LENGTH 100μm

Tech. (nm)	Cu			SWCNT		
	R (KΩ)	***L (nH)***	***C (fF)***	***R (Kohm)***	***L (nH)***	***C (fF)***
16	14.33	0.176	12.537	2.334	1.296	14.11
22	6.21	0.170	14.53	1.220	0.681	12.91
32	2.48	0.163	16.14	0.594	0.301	12.60
45	1.12	0.157	17.37	0.328	0.182	13.50

TABLE III
RLC PARAMETERS OF Cu & SWCNT AT DIFFERENT TECHNOLOGY NODES FOR GLOBAL INTERCONNECT LENGTH 1000μm

Tech. (nm)	Cu			SWCNT		
	R (KΩ)	***L (nH)***	***C (fF)***	***R (Kohm)***	***L (nH)***	***C (fF)***
16	32.918	2.109	135.26	7.823	4.3461	151.666
22	16.40	2.058	154.570	4.540	2.5230	146.660
32	6.365	1.982	172.668	2.065	1.1470	142.954
45	2.957	1.92	189.608	1.102	0.6125	139.330

4 RESULTS AND DISCUSSION

The equivalent interconnect circuit parameter extracted by using Carbon Nanotube Analyzer (CNIA) [9] and Berkeley Predictive Technology Model (BPTM) [10] for SWCNT bundle and Copper interconnect respectively. All the simulation work are done by using Tanner EDA tool.

The interconnect parameters used in this simulation work are obtained from ITRS 2011 as summarized in Table I. In this paper the diameter of individual SWCNT considered as 1nm and width of SWCNT interconnect assumed equal to the spacing between the interconnect.

We considered all the SWCNTs in the bundle are metallic and densely packed. The resistance, inductance and quantum capacitance of SWCNT can be calculated by using equation (13), (14) and (15). The RLC parameters of Copper and SWCNT for intermediate interconnect and global length for different technology nodes are shown in Table II and Table III respectively. The electrostatic capacitance of SWCNTS has slightly different than that of Cu wire. The spacing between the adjacent SWCNTs is assumed to be 0.34nm which is the van der Waals gap.

From the fig4.1and 4.2 it can be inferred that with the advancement of the technology the interconnect delay has been increased because as the technology improve resistivity and chip complexity also increases. It can be observed that for submicron technologies the interconnect delay start to dominate the gate delay [11].

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TABLE IV
DELAY ANALYSIS OF INTERMEDIATE INTERCONNECT OF LENGTH 100µm AT DIFFERENT TECHNOLOGY

Technology (nm)	Delay (pico sec)		Delay ratio of swcnt to Cu
	Cu	*SWCNT*	
16	424.880	368.2887	0.866
22	363.990	323.230	0.888
32	296.972	258.866	0.871
45	245.892	207.940	0.846

TABLE V
DELAY ANALYSIS OF INTERMEDIATE GLOBAL OF LENGTH 1000µm AT DIFFERENT TECHNOLOGY

Technology (nm)	Delay (n sec)		Delay ratio of SWCNT to Cu
	Cu	*SWCNT*	
16	4.136	2.4495	0.5922
22	2.796	1.777	0.6355
32	1.700	1.206	0.7094
45	1.270	0.909	0.7157

TABLE VI
POWER ANALYSIS OF INTERMEDIATE INTERCONNECT OF LENGTH 100µm AT DIFFERENT TECHNOLOGY

Technology (nm)	Power (µW)		Power ratio of SWCNT to Cu
	Cu	*SWCNT*	
16	0.1699	0.18290	1.0765
22	0.2320	0.2249	0.9693
32	0.324	0.2855	0.8811
45	0.4529	0.3777	0.8339

TABLE VII
POWER ANALYSIS OF GLOBAL INTERCONNECT OF LENGTH 1000µm AT DIFFERENT TECHNOLOGY

Technology (nm)	Power (µW)		Power ratio of SWCNT to Cu
	Cu	*SWCNT*	
16	1.2800	1.5211	1.1883
22	2.0060	1.9327	0.9634
32	2.8495	2.3870	0.8376
45	3.8819	2.86512	0.7380

It is observed from the table IV and table V that for different technology the SWCNT interconnect delay is less as compared to Cu for both intermediate and global length of interconnect due to the fact that the Capacitance and resistance associated with the SWCNTs bundle were found to be smaller than that of copper wire of same dimensions as mention in table II and table III.

Fig. 4.3 and 4.4 demonstrated the Power with respect to different technology nodes for intermediate and global level of interconnect respectively. With the advancement of the VLSI technology power dissipation due to interconnect decreases which can be seen from the table VI and table VII, .The result show that for global interconnect both the area and number of SWCNTs in bundle increases, hence equivalent resistance and inductance of the interconnect reduces. Therefore power dissipation of SWCNTs bundle at global level is low as compared to copper interconnect, however an interesting result found at below 22nm technology node which show that SWCNT bundle consume large power as compare to Cu due to increase its capacitance value .

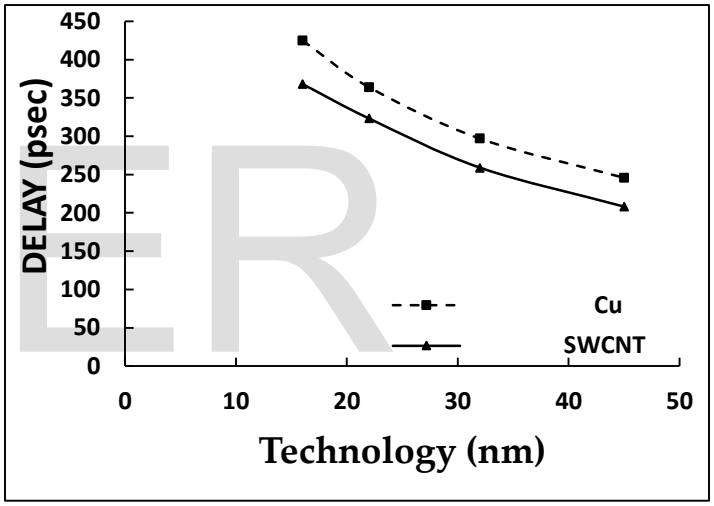

Fig. 4.1. Delay vs Technology (Intermediate Interconect)

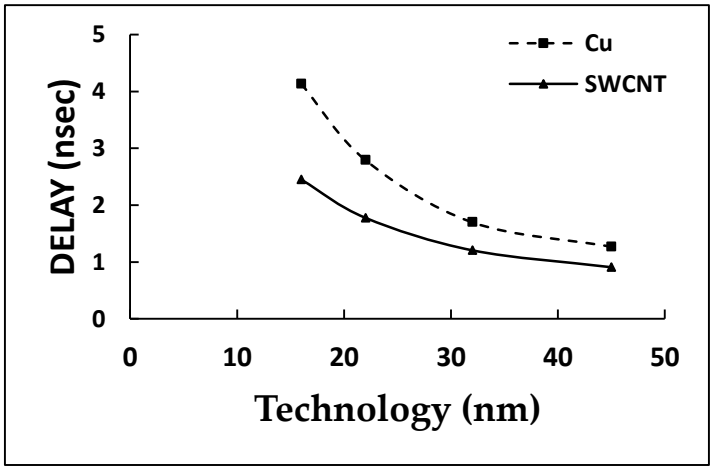

Fig. 4.2. Delay vs Technology (Global Interconnect)

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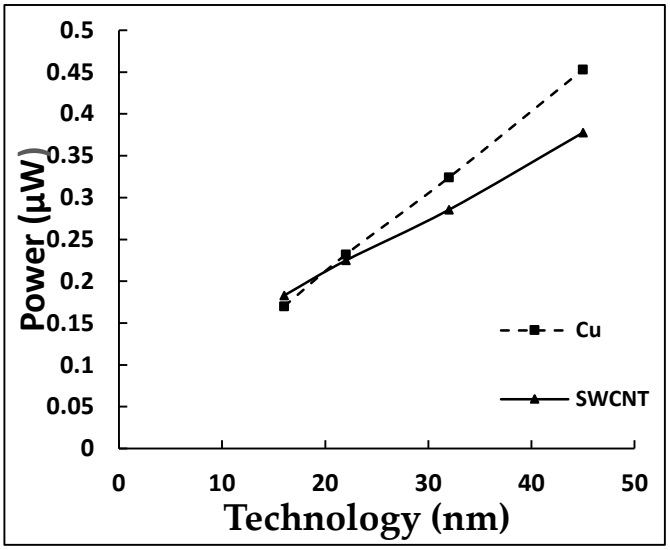

Fig. 4.3. Power vs Technology (Intermediate Interconect)

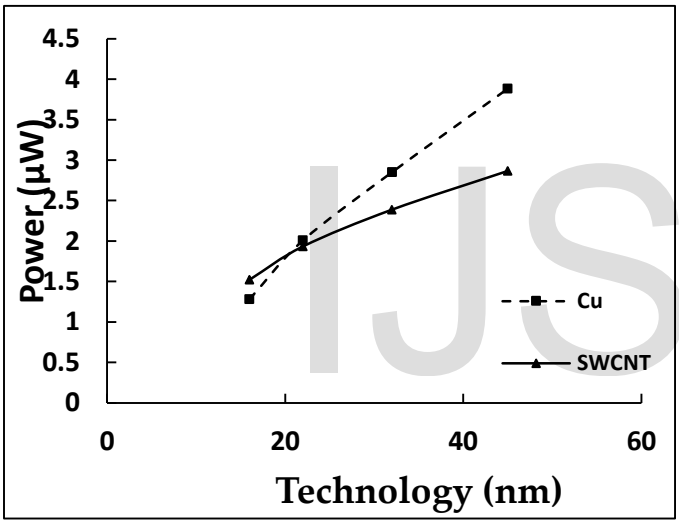

Fig. 4.4. Power vs Technology (Global Interconnect)

5 CONCLUSION

The power dissipation and delay analysis has been performed for both intermediate and global interconnect length at different technology nodes. The result show that with the advancement of technology interconnect delay becomes more prominent, however SWCNT offer less delay as compare to conventional Cu interconnect. It is interesting to observe that below 22nm technology SWCNT bundle interconnect consume almost equal power as by the Cu wire for both intermediate and global level, which restrict the SWCNT bundle as a interconnect at 22nm technology nodes for power constraint design, however it can be concluded that SWCNT bundle is a viable candidate to replace conventional Cu wire for high speed VLSI interconnect based system in future.

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